REMARKS

Applicants respectfully request reconsideration of this application as amended. Claims 17 – 28 have been amended. Claims 29 – 37 have been cancelled. Claims 38 – 49 have been added. Therefore, claims 1 – 28 and 38 – 49 are presented for examination.

In the January 31, 2001 Office Action, claims 1-37 stand rejected under 35 U.S.C. §102(e) as being anticipated by Atkinson, U.S. Patent No. 6,134,167 ("Atkinson"). The rejection with respect to claims 28 – 37 have been obviated due to the cancellation of claims 28 – 37. In addition, Atkinson is not patentable over the remaining claims of the application.

Atkinson discloses refresh logic coupled to a bridge logic device for generating memory refresh signals. See Atkinson at col. 5, ll. 56-60. The refresh logic is also coupled to an external refresh timer and an I/O controller (Figure 2a). Atkinson further discloses that in other embodiments, the refresh logic may be incorporated into the bridge logic device (col. 14, ll. 48-50). Nevertheless, Atkinson does not disclose the refresh logic being incorporated within a memory controller.

Claim 1 recites a memory controller including a refresh timing circuit for generating clock pulses used to trigger memory refresh events. As discussed above, Atkinson discloses refresh logic external to the memory controller. Moreover, Atkinson discloses a clock source that is external to both the refresh logic and the memory controller. As discussed in the applicants' specification, an external clock source requires an additional pin in order to trigger memory refreshes. An additional pin increases circuit

complexity. See Specification at page 3, ll. 12 – 20. Therefore, Claim 1 is patentable over Atkinson.

Because claims 2 – 15 depend from claim 1 and include additional limitations, applicants submit that claims 2 – 15 are also patentable over Atkinson.

Claim 16 recites a memory controller comprising a refresh timing circuit for generating clock pulses used to trigger memory refresh events. Thus, for the reasons stated above with respect to claim 1, claim 16 is also patentable over Atkinson. Since claims 17 – 28 depend from claim 16 and include additional limitations, applicants submit that claims 17 – 28 are also patentable over Atkinson.

New claim 38 is also patentable over Atkinson. Claim 38 recites a refresh timing circuit comprising an internal clock generator. Atkinson does not disclose a refresh timing circuit that includes an internal clock generator. As described above, Atkinson discloses a clock generator that is external to the refresh logic. Consequently, claim 38 is patentable over Atkinson. Because claims 39 – 49 depend from claim 38 and include additional limitations, applicants submit that claims 39 – 49 are also patentable over Atkinson.

It should furthermore be noted that the above amendments to the claims have not been made within view to overcoming any prior art of which the applicants are aware, or that has been cited in the present Office Action. The above amendments have been made with a view to modifying the form of the claims.

Applicants respectfully submit that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for

allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims as amended be allowed.

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Respectfully submitted,

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Claim Versions with Markings to Show Changes Made

16. (Amended) [An Extended Data Out Dynamic Random Access Memory (EDO DRAM)] A memory controller comprising:

a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

17. (Amended) The [computer system] memory controller of claim 16, wherein the refresh timing circuit further comprises:

a clock generator;

a first counter coupled to the clock generator;

a storage register coupled to the clock generator and the counter; and

a comparator coupled to the clock generator, the counter and the storage register.

18. (Amended) The [EDO DRAM] memory controller of claim 17, wherein the [EDO DRAM] memory controller operates in a normal mode and a low power mode.

19. (Amended) The [EDO DRAM] memory controller of claim 18, wherein the first counter counts the number of clock pulses generated by the clock generator.

20. (Amended) The [EDO DRAM] memory controller of claim 19, wherein the first counter transmits data to the storage register whenever the [EDO DRAM] memory

controller is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

21. (Amended) The [EDO DRAM] memory controller of claim 20, wherein the storage register transmits the data to the comparator upon a transition from the normal mode to the low power mode.

22. (Amended) The [EDO DRAM] memory controller of claim 21, wherein the first counter transmits signals to the comparator whenever the [EDO DRAM] memory controller is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

23. (Amended) The [EDO DRAM] memory controller of claim 22, wherein the comparator compares the signal received from the first counter and the data received from the storage register, and wherein the comparator transmits a refresh trigger signal whenever there is a match between the signal and the data.

24. (Amended) The [EDO DRAM] memory controller of claim 19, wherein the refresh timing circuit further comprises a second counter.

25. (Amended) The [EDO DRAM] memory controller of claim 24, wherein the first counter counts the number of clock pulses generated by the clock generator while the [EDO DRAM] memory controller is operating in the low power mode and the second counter counts the number of clock pulses generated by the clock generator while the [EDO DRAM] memory controller is operating in the normal mode.

26. (Amended) The [EDO DRAM] memory controller of claim 25, wherein the second counter transmits data to the storage register upon the occurrence of a memory refresh event whenever the [EDO DRAM] memory controller is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

27. (Amended) The [EDO DRAM] memory controller of claim 26, wherein the second counter is deactivated and the first counter is activated whenever the [EDO DRAM] memory controller transitions from the normal mode to the low power mode.

28. (Amended) The [EDO DRAM] memory controller of claim 27, wherein the first counter transmits signals to the comparator whenever the [EDO DRAM] memory controller is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

29-37. (Cancelled)

38. (New) --A refresh timing circuit comprising:

an internal clock generator;

a first counter coupled to the clock generator;

a storage register coupled to the clock generator and the counter; and

a comparator coupled to the clock generator, the counter and the storage register.

39. (New) The refresh timing circuit of claim 38, wherein the refresh timing circuit operates in a normal mode and a low power mode.

40. (New) The refresh timing circuit of claim 39, wherein the first counter counts the number of clock pulses generated by the clock generator.

41. (New) The refresh timing circuit of claim 40, wherein the first counter transmits data to the storage register whenever the refresh timing circuit is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

42. (New) The refresh timing circuit of claim 41, wherein the storage register transmits the data to the comparator upon a transition from the normal mode to the low power mode.

43. (New) The refresh timing circuit of claim 42, wherein the first counter transmits signals to the comparator whenever the refresh timing circuit is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.

44. (New) The refresh timing circuit of claim 43, wherein the comparator compares the signal received from the first counter and the data received from the storage register, and wherein the comparator transmits a refresh trigger signal whenever there is a match between the signal and the data.

45. (New) The refresh timing circuit of claim 40, further comprising a second counter.

46. (New) The refresh timing circuit of claim 45, wherein the first counter counts the number of clock pulses generated by the clock generator while the refresh timing circuit is operating in the low power mode and the second counter counts the number of clock

pulses generated by the clock generator while the refresh timing circuit is operating in the normal mode.

47. (New) The refresh timing circuit of claim 46, wherein the second counter transmits data to the storage register upon the occurrence of a memory refresh event whenever the refresh timing circuit is operating in the normal mode, the data representing the number of clock pulses counted by the counter since the occurrence of a previous memory refresh event.

48. (New) The refresh timing circuit of claim 47, wherein the second counter is deactivated and the first counter is activated whenever the refresh timing circuit transitions from the normal mode to the low power mode.

49. (New) The refresh timing circuit of claim 48, wherein the first counter transmits signals to the comparator whenever the refresh timing circuit is operating in the low power mode, the signal representing the number of clock pulses received from the clock generator.--